

H7N1005LD, H7N1005LS, H7N1005LM

Silicon N Channel MOS FET High Speed Power Switching

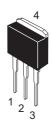
REJ03G0391-0200 Rev.2.00 Oct 16, 2006

Features

- Low on-resistance $R_{DS (on)} = 85 \text{ m}\Omega \text{ typ.}$
- Low drive current
- Capable of 4.5 V gate drive

Outline

RENESAS Package code: PRSS0004AE-A (Package name: LDPAK (L))



H7N1005LD

RENESAS Package code: PRSS0004AE-C (Package name: LDPAK (S)-(2))



H7N1005LM

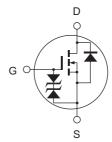
RENESAS Package code: PRSS0004AE-B (Package name: LDPAK (S)-(1))



H7N1005LS

1. Gate 2. Drain

3. Source 4. Drain



Absolute Maximum Ratings

 $(Ta = 25^{\circ}C)$

Item	Symbol	Value	Unit
Drain to source voltage	V_{DSS}	100	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	15	A
Drain peak current	I _{D (pulse)} Note 1	30	A
Body to drain diode reverse drain current	I _{DR}	30	A
Avalanche current	I _{AP} Note 3	8	А
Avalanche energy	E _{AR} Note 3	6.4	mJ
Channel dissipation	Pch Note 2	30	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	−55 to +150	°C

Notes: 1. PW \leq 10 μ s, duty cycle \leq 1%

2. Value at Tc = 25°C

3. Value at Tch = 25°C, Rg \geq 50 Ω

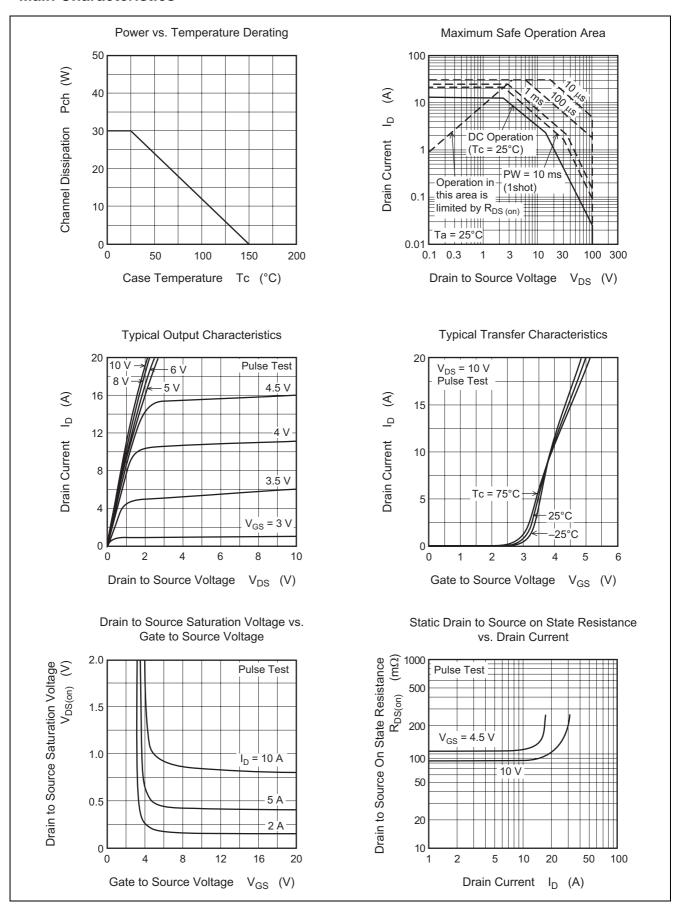
Electrical Characteristics

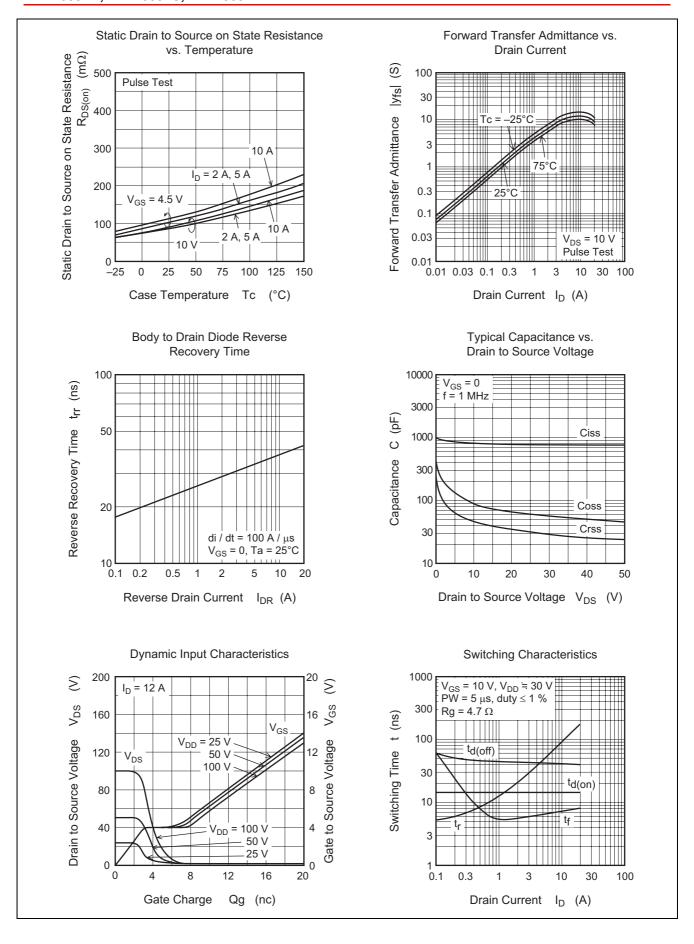
 $(Ta = 25^{\circ}C)$

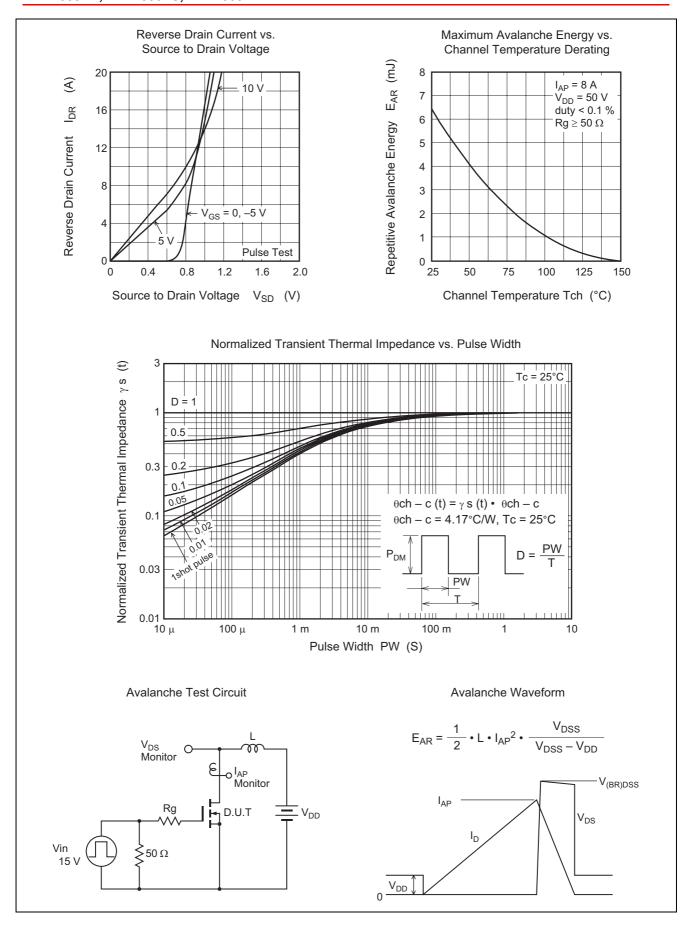
Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR) DSS}	100	_	_	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20		_	V	$I_G = \pm 100 \ \mu A, \ V_{DS} = 0$
Gate to source leak current	I _{GSS}	_		±10	μΑ	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I _{DSS}	_		10	μΑ	$V_{DS} = 100 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	V _{GS (off)}	1.5		2.5	V	$I_D = 1 \text{ mA}, V_{DS} = 10 \text{ V}^{\text{Note 4}}$
Static drain to source on state	R _{DS (on)}	_	85	110	mΩ	$I_D = 7.5 \text{ A}, V_{GS} = 10 \text{ V}^{\text{Note 4}}$
resistance		_	105	155	mΩ	$I_D = 7.5 \text{ A}, V_{GS} = 4.5 \text{ V}^{\text{Note 4}}$
Forward transfer admittance	y _{fs}	6.5	11	_	S	$I_D = 7.5 \text{ A}, V_{GS} = 10 \text{ V}^{\text{Note 4}}$
Input capacitance	Ciss	_	830	_	pF	V _{DS} = 10 V
Output capacitance	Coss	_	90	_	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	_	55	_	pF	f = 1 MHz
Total gate charge	Qg	_	15	_	nC	V _{DD} = 50 V
Gate to source charge	Qgs	_	3	_	nC	V _{GS} = 10 V
Gate to drain charge	Qgd	_	4	_	nC	I _D = 15 A
Turn-on delay time	t _{d (on)}	_	15	_	ns	$V_{GS} = 10 \text{ V}, I_D = 7.5 \text{ A}$
Rise time	t _r	_	85	_	ns	$R_L = 4 \Omega$
Turn-off delay time	t _{d (off)}	_	42	_	ns	$Rg = 4.7 \Omega$
Fall time	t _f	_	6.8	_	ns	
Body to drain diode forward voltage	V_{DF}	_	0.93	_	V	I _F = 15 A, V _{GS} = 0
Body to drain diode reverse recovery	t _{rr}	_	41	_	ns	I _F = 15 A, V _{GS} = 0
time						$di_F/dt = 100 A/\mu s$

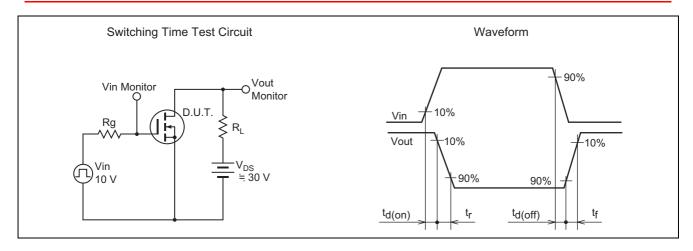
Note: 4. Pulse test

Main Characteristics

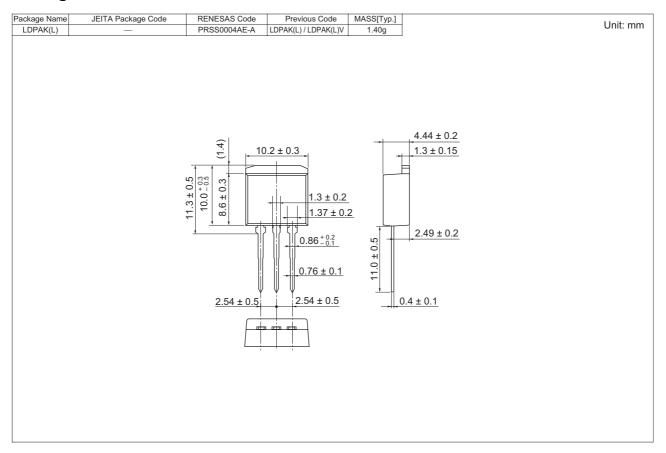


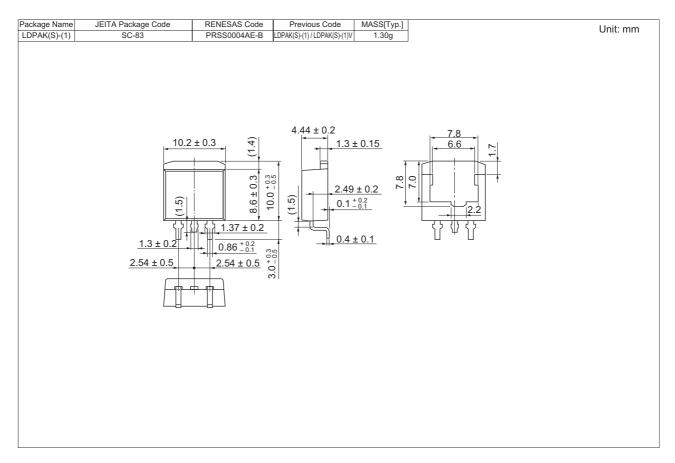


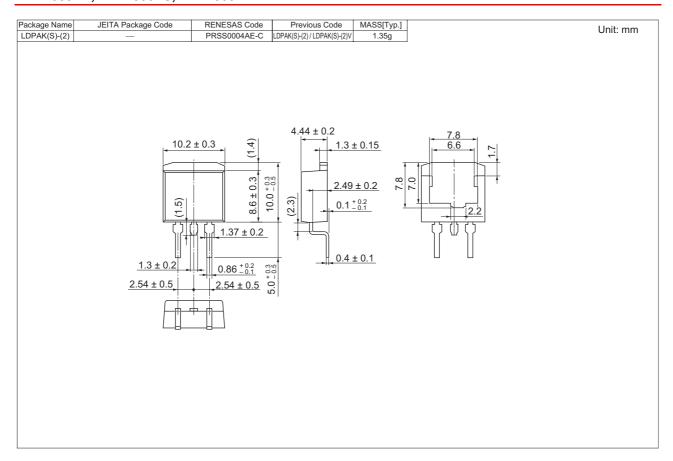




Package Dimensions







Ordering Information

Part Name	Quantity	Shipping Container
H7N1005LD-E	500 pcs	Box (Conductive Sack)
H7N1005LSTL-E	1000 pcs	Taping
H7N1005LMTL-E	1000 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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